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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,871	06/29/2001	Thomas D. Fletcher	2207/11273	6547
23838	7590	07/23/2004	EXAMINER	
KENYON & KENYON 1500 K STREET, N.W., SUITE 700 WASHINGTON, DC 20005			DU, THUAN N	
			ART UNIT	PAPER NUMBER
			2116	
DATE MAILED: 07/23/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/893,871

Applicant(s)

FLETCHER ET AL.

Examiner

Thuan N. Du

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

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Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/28/02</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS (dated 2/28/02).
2. Claims 1-27 are presented for examination.

Claim Objections

3. Claim 8 is objected to because of the following informalities: "an delay" in line 10 should be -- a delay --. Appropriate correction is required.
4. Claims 9-11 are also objected for incorporating the above deficiency by dependency.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Heffner et al. [Heffner] (U.S. Patent No. 3,921,079).

7. Regarding claim 1, Heffner teaches a circuit comprising:

a plurality of outputs (terminals 14, 16; A1-An, B1-Bn) to provide a sequence of clock signals which together comprises a multistage clock [Fig. 1; col. 2, lines 40-60; col. 5, lines 37-53]; and

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a delay adjustment input (50) to adjust the timing of the clock signals for at least one of the outputs [col. 3, lines 41-50; col. 4, lines 24-31] relative to the clock signals at another of the outputs [col. 6, lines 1-14, 24-33].

8. Regarding claim 2, Heffner teaches that the delay adjustment input adjusts the timing of the clock signal at said one output and at all of the outputs that follow said one output in the multistage clock, wherein said adjustment are relative to the output that precedes said one output in the multistage clock [col. 6, lines 24-33].

9. Regarding claim 3, Heffner teaches that the circuit has a plurality of said adjustment inputs (the inputs to the plurality of phase shift adjust means) [Fig. 1].

10. Regarding claim 4, Heffner teaches a circuit comprising:

a clock input to receive a clock input signal [Fig. 1; col. 2, line 30];

a plurality of clock outputs (terminals 14, 16; A1-An, B1-Bn) to each provide a delayed version of the clock input signal [col. 2, lines 43-49], wherein the amount of delay in the signal at each of the clock outputs differs from the amount of delay in the signal at the other clock outputs by approximately a multiple of a time t [col. 6, lines 1-14, 24-33]; and

a delay adjustment block (phase shift adjust means) to vary the difference in the amount of delay in the signal at one of the clock outputs compared to the signal at another of the clock outputs [col. 3, lines 5-14; col. 4, lines 24-31].

11. Regarding claim 5, Heffner teaches that the delay adjustment block has an input to digitally control the variation in the amount of delay [Fig. 1; col. 6, lines 24-33].

12. Regarding claim 6, Heffner teaches that the circuit has a plurality of said delay adjustment blocks (phase shift adjust means 24-30) [Fig. 1], wherein the clock outputs

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have a sequential order [Fig. 5], and wherein each of the delay adjustment blocks varies the delay between a clock output and all of the clock outputs that follow that output in the sequential order [col. 6, lines 24-33].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heffner et al. [Heffner] (U.S. Patent No. 3,921,079).

15. Regarding claim 7, Heffner does not explicitly teach that the time t is approximately the delay of an inverter with a fanout of 2. However, it is a matter of design choice to implement the amount of delay.

16. Regarding claims 8-11, Heffner teaches a circuit comprising:

a clock input [Fig. 1; col. 2, line 30];

a plurality of clock outputs (terminals 14, 16; A1-An, B1-Bn) each connected by a path to the clock input [Fig. 1];

a plurality of first delay blocks (circuits 24-30) each of which is part of a single path from the clock input to one of the clock outputs (paths 12-A1, 12-A2 ... 12-Bn)

[Fig. 1]; and

a plurality of second delay blocks (circuits 70-76) each of which is part of one of said paths from the clock input to a clock output through one of the first delay blocks

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(paths 12-A1, 12-A2 ... 12-Bn) and is part of another path from the clock input to another clock output through another first delay block (circuit 70 is in a different path of circuit 26) [Fig. 1].

Heffner does not explicitly teach a delay adjustment block connected to an output of one of the second delay blocks.

However, one of ordinary skill in the art would have recognize that it would have been obvious for the delay adjustment block to connect to an output of one of the second delay blocks because it would increase the accuracy for determining the amount of delay.

17. Regarding claims 19-23, Heffner teaches a circuit comprising:

a clock input [Fig. 1; col. 2, line 30];

a plurality of chain of two inverters (inverters 17-22 of Fig. 1 and inverter 98, shown in Fig. 4, in each of circuits 70-76) having an input connected to said clock input and having an output connected to clock outputs [Fig. 1].

18. Regarding claims 12-18 and 24-27, since they recite method of operating of the apparatus defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (703) 308-6292. The examiner can normally be reached on Monday-Friday: 9:00 AM - 5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (703) 308-1159.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

The fax number for the organization is (703) 872-9306.

A handwritten signature in black ink, appearing to read 'Thuan N. Du', with a stylized flourish at the end.

Thuan N. Du
July 20, 2004

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